

REMARKS

Claims 1-3, 5-8, and 32-41 are pending in this application. For purposes of expedition, claims 1, 5, 6, 8, 32, 34, 35, 38, 39 and 40 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

Claims 1-3, 5-8 and 32-41 have been rejected under 35 U.S.C. §112, 2d ¶, as being indefinite. Specifically, the Examiner questions the meaning of the phrase "interleaving the data from the plurality of the partitions so that partitions from each of the ECC blocks are alternately selected such that progression through the partitions of each ECC block occurs diagonally to generate a first recording block" as defined in base claim 1. The Examiner further asserts that such a phrase is so ambiguous, imprecise and indefinite and so open to so many interpretations, including those presented on pages 2-3 of the Office Action (Paper No. 20051003). However, the Examiner's many interpretations are not correct. Data is not interleaved by alternately selecting the ECC blocks that are combined to form a group of ECC blocks, or alternatively, by alternately selecting the ECC blocks that are combined to form a combined block of ECC blocks, as suggested by the Examiner. Rather, as clearly explained in Applicants' specification, ¶0023 described in connection with FIG. 1B, data is interleaved by way of alternately extracting data from partitions from each of the ECC blocks so that each of the ECC blocks is alternately selected. The definiteness of the language employed must be analyzed not in a vacuum, but in light of the teachings in the prior art and of the particular application disclosure as it would be interpreted by one skilled in the art. In re Angstadt, 537 F.2d 498, 190 USPQ 214, 217 (CCPA 1976). When interpreted in view of Applicants' disclosure, the phrase in question is clearly definite. Nevertheless, in the interest of expedition, base claim 1 has been amended to overcome any question of ambiguity.

In addition, the Examiner also questions the meaning of the phrase "interleaving the data from the partitions, comprising alternately selecting the partitions of each of the ECC blocks along diagonal paths" as defined in base claim 32. For purposes of expedition, base claim 32 has been amended to render the rejection moot.

In view of the foregoing explanations, amendments to claims 1 and 32, and the text provided from Applicants' disclosure, Applicants respectfully request that the rejection of claims 1

and 32 be withdrawn.

Claims 1-3, 5-8 and 32-41 have been rejected under 35 U.S.C. §102(e) as being anticipated by Noda, U.S. Patent No. 6,216,245 B1 for the same reasons stated on pages 7-16 of the Office Action (Paper No. 20041108) dated on November 16, 2004 and previously issued in connection with the original application. For example, in support of the rejection of base claims 1 and 32, the Examiner asserts that Noda '245 discloses,

"dividing each of a plurality of error correction code (ECC) blocks into a plurality of partitions (Figure 5 in Noda teaches dividing each of a plurality of error correction code (ECC) blocks into 16 sector partitions); and interleaving the data from the partitions so that each of the FCC blocks is alternately and equally selected to generate a first recording block (Figure 8 in Noda teaches interleaving the data from the sector partitions so that each of the ECC blocks is delayed and alternately and equally selected to generate first recording blocks depicted in the rows of Figure 9 in Noda)." See pages 7-8 and pages 14-15 of Paper No. 20041108, dated on November 16, 2004.

Further, in response to Applicants' discussions of how Noda '245 only discloses dividing an ECC block in a row direction, as shown in FIG. 5, and does not disclosing any division of an ECC block in a column direction, as presented in the Amendment After Final dated on August 10, 2005, the Examiner further argues, on pages 9-10 of the Office Action (Paper No. 20051003), that,

"FIG. 5 in Noda teaches each ECC block is divided into 208 rows and 182 byte columns. The 16 sectors partitions of each ECC block is formed using 16 rows and 182 byte columns; hence Noda explicitly teaches dividing each of a plurality of error correction code (ECC) blocks corresponding to the data in Figures 1 and 5 into a plurality of sector partitions which are formed by dividing each ECC block into 208 rows and 182 byte columns in row and column directions and constructing the sector partitions using 16 rows and 182 byte columns from 208 rows and 182 byte columns.

No matter how the Applicant spins it, the sector partitions are still formed from the 208 rows and 182 byte columns; hence they are still formed by dividing each ECC block into 208 rows and 182 byte columns."

However, the Examiner's assertions are factually incorrect, and legally improper. Applicants submit that the partitioning of an ECC block in both row and column directions to form a plurality of partitions and the extraction of data from those partitions prior to interleaving

are not disclosed or suggested anywhere in Noda '245. Therefore, Applicants traverse the rejection and respectfully request the Examiner to reconsider and withdraw this rejection for the following reasons.

First of all, base claims 1 and 32 have been amended to establish the relationship between an ECC block and a plurality of partitions, and to clearly define that each ECC block has a predetermined size of rows and columns, i.e., N1 bytes of data (row) and N2 bytes of data (column) as shown in FIG. 2A, and that each ECC is further divided both in row and column directions to form a plurality of partitions, in which each partition has a predetermined unit in row and column directions, for example, Partition 1_1, Partition 2-1... Partition d_1 (see 1st row of an ECC block "A" shown in FIG. 2A), and Partition 1_1, Partition d_3 ... Partition 2_2d-1 (see 1st column of an ECC block "A" shown in FIG. 2A).

In contrast to Applicants' base claims 1 and 32, Noda '245 discloses a different interleaving process, one in which input data is also encoded with ECC to generate an ECC block, as shown in FIG. 5, having a size of 172 bytes (in row) and 192 bytes (in column). An inner code parity of 10 bytes and an outer code parity of 16 bytes are further added so that each ECC block is provided with 182 bytes (in row) and 208 bytes (in column). Each ECC block is then further divided, but only in a **row direction**. Specifically, as shown in FIG. 6, each ECC block is divided into 16 (0-15) partitions in the **row direction**. Each of the partitions now has the same 182 bytes (in row), but now has a significantly lower byte count in column, i.e., 12 bytes (obtained by dividing 16 partitions from the original 192 bytes).

As can be seen from FIG. 5, and in contrast to Applicants' base claims 1 and 32, the ECC block of Noda '245 is **not** divided in a **column direction**, as asserted by the Examiner. FIG. 5 of Noda '245 does **not** teach that each ECC is divided into 208 rows and 182 columns, as mistakenly believed by the Examiner. Rather, FIG. 5 of Noda '245 simply shows the size of an ECC block of 172 bytes in row and 192 bytes in column, and that the ECC block can be divided into 16 partitions along a row direction, where each partition is provided with the same 172 bytes in row, but only 12 bytes in column. In fact, the Examiner's own rationale provided on pages 9-10 of the Office Action (Paper No. 20051003) undermines his assertion. Specifically, the Examiner asserts that,

"Noda explicitly teaches dividing each of a plurality of error correction code (ECC) blocks corresponding to the data in Figures 1 and 5 into a plurality of sector partitions which are formed by dividing each ECC block into 208 rows and 182 byte columns in row and column directions and constructing the sector partitions using 16 rows and 182 byte columns from 208 rows and 182 byte

columns."

However, such an assertion is factually incorrect. This is because, if the partition is formed from an ECC block having the same 182 bytes in a row direction as the ECC block, then the same 182 bytes in a row direction has not been divided in a column direction, as required by Applicants' base claims 1 and 32.

As the Examiner can appreciate, the rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

The burden of establishing a basis for denying patentability of a claimed invention rests upon the Examiner. The limitations required by the claims cannot be ignored. See In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). All claim limitations, including those which are functional, must be considered. See In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981). Hence, all words in a claim must be considered in deciding the patentability of that claim against the prior art. Each word in a claim must be given its proper meaning, as construed by a person skilled in the art. Where required to determine the scope of a recited term, the disclosure may be used. See In re Barr, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

In the present situation, Noda '245 fails to disclose and suggest key features of Applicants' base claims 1 and 32 and their respective dependent claims. Therefore, Applicants respectfully request that the rejection of claims 1-3, 5-8 and 32-41 be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC office at (202) 216-9505 ext. 232. Applicants respectfully reserve all rights to file subsequent related application(s) (including reissue applications) directed to any or all

previously claimed limitations/features which have been amended or canceled, or to any or all limitations/features not yet claimed, i.e., Applicants have no intention or desire to dedicate or surrender any limitations/features of the disclosed invention to the public.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. attorney at the local Washington, D.C. telephone number (202) 216-9505 ext. 232 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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